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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,981	09/22/2003	Chun-Chi Lee	LEEC3073/EM	4969

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EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,981	LEE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I in the reply filed on June 16, 2004 is acknowledged.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

3. Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in Serial No. 09220880620 on September 22, 2003. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application. A new oath, declaration or application data sheet is required in the body of which the present application should be identified by application number and filing date.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim 15 limitation "wherein the conductive devices are conductive wires, and the back surface of the semiconductor chip faces and connects to the upper surface of the substrate via the thermal enhance layer." must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations

indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Marked-up Drawings" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 7, 10, 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Weaver et al. (U. S. Pat. No. 6,117,352).

Regarding claim 1, Weaver et al. discloses in e.g., Fig. 1 and Fig. 4 a semiconductor package, comprising:

- a substrate (14) having an upper surface and a lower surface opposed to the upper surface;
- a semiconductor chip (12) having an active surface (at the surface that has pads), a back surface opposed to the active surface and a plurality of bonding pads (20) formed on the active surface;

- a plurality of conductive devices (22), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and
- a thermal enhance layer (34, at the bottom; Fig. 4 and column 2, line 11) formed on the back surface of the semiconductor chip.

Regarding claim 2, Weaver et al. discloses in e.g., Fig. 4 further comprising an underfill (34, at the top; Fig. 4) disposed between the active surface of the semiconductor chip and the upper surface of the substrate.

Regarding claim 3, Weaver et al. discloses in e.g., Fig. 4 and column 6, lines 48 – 51 a material of the thermal enhance layer (34; epoxy which is a polymer) comprising thermally conductive polymer layer.

Regarding claim 4, Weaver et al. discloses in e.g., Fig. 4 and column 6, lines 48 – 51 a material of the thermally conductive polymer layer (34; epoxy which is a polymer and a film) comprising thermally conductive film.

Regarding claim 5, Weaver et al. discloses in e.g., Fig. 4 and column 6, lines 48 – 51 a material of the thermally conductive polymer layer (34; epoxy) comprising thermally conductive epoxy.

Regarding claim 6, Weaver et al. discloses in e.g., Fig. 1 and Fig. 4 further comprising a heat spreader (30) attached on the thermal enhance layer (34, at the bottom in Fig. 4).

Regarding claim 7, Weaver et al. discloses in e.g., Fig. 1 and Fig. 4 the heat spreader (30) being a flat heat spreader.

Regarding claim 10, Weaver et al. discloses in e.g., Fig. 1, Fig. 4 and column 6, lines 41 – 43 a material of the heat spreader (30; Cu) comprising copper.

Regarding claim 14, Weaver et al. discloses in e.g., Fig. 1 and Fig. 4 the conductive devices (22) being conductive bumps (solder bumps; column 6, line 3), and the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps (see Figs. 1 and 4).

Regarding claim 17, Weaver et al. discloses in e.g., Fig. 1 and Fig. 4 further comprising a plurality of solder balls (24; column 6, line 22) formed on the lower surface of the substrate.

8. Claims 1, 2, 6, 11, 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushima (U. S. Pat. No. 6,184,586).

Regarding claim 1, Matsushima discloses in e.g., Fig. 8(c) a semiconductor package, comprising:

- a substrate (1) having an upper surface and a lower surface opposed to the upper surface;
- a semiconductor chip (2) having an active surface (at the surface that has pads), a back surface opposed to the active surface and a plurality of bonding pads (the pads under the elements 5) formed on the active surface;
- a plurality of conductive devices (5), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and

- a thermal enhance layer (7b and column 1, lines 60 – 62) formed on the back surface of the semiconductor chip.

Regarding claim 2, Matsushima discloses in e.g., Fig. 8(c) further comprising an underfill (8) disposed between the active surface of the semiconductor chip and the upper surface of the substrate.

Regarding claim 6, Matsushima discloses in e.g., Fig. 8(c) further comprising a heat spreader (3) attached on the thermal enhance layer (7b).

Regarding claim 11, Matsushima discloses in e.g., Fig. 8(c) further comprising a stiffener ring (4) connecting the substrate and the heat spreader.

Regarding claim 14, Matsushima discloses in e.g., Fig. 8(c) the conductive devices (5) being conductive bumps (solder bumps; column 2, line 33), and the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps (see Fig. 8(c)).

Regarding claim 17, Matsushima discloses in e.g., Fig. 8(c) further comprising a plurality of solder balls (6; column 1, line 32) formed on the lower surface of the substrate.

9. Claims 1, 2, 6, 8 – 10, 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by McCormick et al. (U. S. Pat. No. 5,909,057).

Regarding claim 1, McCormick et al. discloses in e.g., Fig. 2F a semiconductor package, comprising:

- a substrate (206) having an upper surface and a lower surface opposed to the upper surface;

- a semiconductor chip (200) having an active surface (at the surface that has pads), a back surface opposed to the active surface and a plurality of bonding pads (the pads under the elements 204) formed on the active surface;
- a plurality of conductive devices (204), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and
- a thermal enhance layer (a thermally conductive thermal adhesive between the chip and the heat spreader; column 7, lines 16 – 21) formed on the back surface of the semiconductor chip.

Regarding claim 2, McCormick et al. discloses in e.g., Fig. 2F further comprising an underfill (208) disposed between the active surface of the semiconductor chip and the upper surface of the substrate.

Regarding claim 6, McCormick et al. discloses in e.g., Fig. 2F further comprising a heat spreader (210; see Fig. 2B) attached on the thermal enhance layer (a thermally conductive thermal adhesive and column 7, lines 16 – 21).

Regarding claim 8, McCormick et al. discloses in e.g., Fig. 2F the spreader (210) being a cap-like heat spreader (see Fig. 2B).

Regarding claim 9, McCormick et al. discloses in e.g., Fig. 2F further comprising an adhesive (a thermally conductive thermal adhesive between the substrate and the heat spreader; column 7, lines 16 – 21) connecting the substrate and the heat spreader.

Regarding claim 10, McCormick et al. discloses in e.g., Fig. 2F and column 6, lines 24 – 29 a material of the heat spreader (210; Ni-plated Cu) comprising copper.

Regarding claim 14, McCormick et al. discloses in e.g., Fig. 2F the conductive devices (204) being conductive bumps (solder bumps; column 7, line 9), and the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps (see Fig. 2F).

Regarding claim 17, McCormick et al. discloses in e.g., Fig. 2F further comprising a plurality of solder balls (230) formed on the lower surface of the substrate.

10. Claims 1, 3 – 5, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Karnezos (U. S. Pat. No. 5,397,921).

Regarding claim 1, Karnezos discloses in e.g., Fig. 2a a semiconductor package (353), comprising:

- a substrate (106 and 203) having an upper surface and a lower surface opposed to the upper surface;
- a semiconductor chip (101) having an active surface (at the surface that connected to the wire 210a and 210b), a back surface opposed to the active surface and a plurality of bonding pads (the pads under the elements 210a and 210b) formed on the active surface;
- a plurality of conductive devices (210a and 210b), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and
- a thermal enhance layer (105; column 4, lines 64 – 65) formed on the back surface of the semiconductor chip.

Regarding claim 3, Karnezos discloses in e.g., Fig. 2a and column 4, lines 64 – 65 a material of the thermal enhance layer (105; epoxy which is a polymer) comprising thermally conductive polymer layer.

Regarding claim 4, Karnezos discloses in e.g., Fig. 2a and column 4, lines 64 – 65 a material of the thermally conductive polymer layer (105; epoxy which is a polymer and a film) comprising thermally conductive film.

Regarding claim 5, Karnezos discloses in e.g., Fig. 2a and column 4, lines 64 – 65 a material of the thermally conductive polymer layer (34; epoxy) comprising thermally conductive epoxy.

Regarding claim 15, Karnezos discloses in e.g., Fig. 2a the conductive devices (210a and 210b; column 8, line 8) being conductive wires, and the back surface of the semiconductor chip faces and connects to the upper surface of the substrate via the thermal enhance layer.

Regarding claim 16, Karnezos discloses in e.g., Fig. 2a the substrate (106 and 203) having an opening (the cavity or opening where the chip is located) and the semiconductor chip is disposed in the opening.

11. Claims 1, 6, 14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozawa (U. S. Pat. No. 5,471,366).

Regarding claim 1, Ozawa discloses in e.g., Fig. 11 a semiconductor package (120), comprising:

- a substrate (121a – 121c) having an upper surface and a lower surface opposed to the upper surface;

- a semiconductor chip (32-1) having an active surface (at the surface that forms the bumps), a back surface opposed to the active surface and a plurality of bonding pads (the pads under the bumps) formed on the active surface;
- a plurality of conductive devices (the bumps), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and
- a thermal enhance layer (33-1; column 4, line 65 – column 5, line 5) formed on the back surface of the semiconductor chip.

Regarding claim 6, Ozawa discloses in e.g., Fig. 11 further comprising a heat spreader (36) attached on the thermal enhance layer (33-1).

Regarding claim 14, Ozawa discloses in e.g., Fig. 11 the conductive devices (the bumps) being conductive bumps, and the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps (see Fig. 11).

Regarding claim 18, Ozawa discloses in e.g., Fig. 11 further comprising an additional semiconductor chip (122 - 1) attached on the lower surface of the substrate.

12. Claims 1, 6, 8, 12 – 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (U. S. Pat. No. 5,777,385).

Regarding claim 1, Wu discloses in e.g., Fig. 1 and Fig. 2 a semiconductor package (10 and 20), comprising:

- a substrate (14) having an upper surface and a lower surface opposed to the upper surface;

- a semiconductor chip (13) having an active surface (at the surface that forms the bumps 29 or 15), a back surface opposed to the active surface and a plurality of bonding pads (the pads under the bumps 29 and 15) formed on the active surface;
- a plurality of conductive devices (the bumps 29 and 15), the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; and
- a thermal enhance layer (12 and column 2, line 47 – 48; and 28 and column 3, lines 19 – 20) formed on the back surface of the semiconductor chip.

Regarding claim 6, Wu discloses in e.g., Fig. 1 and Fig. 2 further comprising a heat spreader (11 in Fig. 1 and 21 in Fig. 2) attached on the thermal enhance layer (12 in Fig. 1 and 28 in Fig. 2).

Regarding claim 8, Wu discloses in e.g., Fig. 1 the spreader (11) being a cap-like heat spreader (see Fig. 1).

Regarding claim 12, Wu discloses in e.g., Fig. 2 coefficient of the thermal expansion of the heat spreader being "substantially" the same as that of the semiconductor chip (column 3, lines 30 – 33).

Regarding claim 13, Wu discloses in e.g., Fig. 2 a material of the heat spreader (Si; column 3, line 30) comprising silicon.

Regarding claim 14, Wu discloses in e.g., Fig. 2 the conductive devices (29 in Fig. 2 and 15 in Fig. 1) being conductive bumps (solder bumps; column 3, line 21), and the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps (see Figs. 1 and 2).

Regarding claim 17, Wu discloses in e.g., Fig. 2 further comprising a plurality of solder balls (16; column 2, line 47) formed on the lower surface of the substrate.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Banks et al., Desai et al., Covell, II et al., Caletka et al., Kim et al. and Toy et al. disclose a semiconductor and a heat sink.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

Tom Thomas

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c.c.
Wednesday, September 15, 2004